A 6 GHz, 50 Watt Low Distortion Push-Pull GaAs Power FET Optimized for 12V Class A-B Operation

T.Yamamoto, S.Sano, K.Naito, T.Igarashi and J.Fukaya

FUJITSU QUANTUM DEVICES LIMITED
Kokubo-Kogyo-Danchi, Showa-Chou Nakakoma-Gun Yamanashi-Ken 409-3883, JAPAN

Abstract **A low distortion 50 Watt push-pull quasi E-mode GaAs FET for 6 GHz terrestrial and satellite communication applications has been developed. The push-pull FET, which operates at drain voltage (V_{ds}) of 12 V, class A-B, has a saturated output power (P_{sat}) of 47 dBm (50 W) and a linear gain (G_L) of 10 dB in the frequency range of 5.8 to 6.5 GHz. A third order intermodulation distortion (IM_3) and an associated power-added efficiency (PAE) at 41 dBm output power of -35 dBc and 18 % respectively. As compared with conventional single-ended D-mode FET, it has an IM_3 and PAE improvement of 5 dB and 5 % respectively.**

INTRODUCTION

High power and low distortion performance are requested for the C-band high capacity SDH radio link system. Especially, high efficiency at operating point is the key issue. The class A operated single-ended D-mode FETs are used conventionally. However, when they are operated at Class A-B to enhance the PAE or to decrease the channel temperature, the degradation of IM_3 can not be avoided. Most of SDH radio link systems use linearization to satisfy the system specifications, which requires an IM_3 of –35 dBc for the final stage devices. It is important to obtain an appropriate IM_3 for the systems in Class A-B operation.

Recently, for L- and S-band cellular base station application, over 100 W GaAs push-pull FETs using quasi E-mode chips have been successfully developed with a high efficiency and a low distortion [1,2,3]. However, there are no reports about C-band high power quasi E-mode FETs. This paper demonstrates a 6 GHz 50W low distortion push-pull GaAs power FET optimized for 12 V Class A-B operation.

FET CHIP STRUCTURE AND CHARACTERISTICS

The optimized quasi E-mode FET chip consists of a Si doped GaAs channel layer, AlGaAs Schottky layer, and a WSi/Au T-shaped gate. The wafer was thinned to 28 μm and a 40-μm gold layer was plated on the backside. The geometry of the device electrodes was determined by considering the RF performance at C-band and the thermal resistance. The drain-to-gate breakdown voltage was higher than 25 V, which was sufficient to operate at 12V drain voltage.

Fig.1. shows the comparison of IM_3 dependence on PAE for D-mode and quasi E-mode FETs. The FET performance was measured at 6 dB back-off from the saturated output power. Both FETs, which have a total gate width of 1.0 mm, were operated at V_{ds}=12V. When conventional D-mode FET was operated at Class A-B bias point to enhance the power-added efficiency, the IM_3 could not meet the system criteria.

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

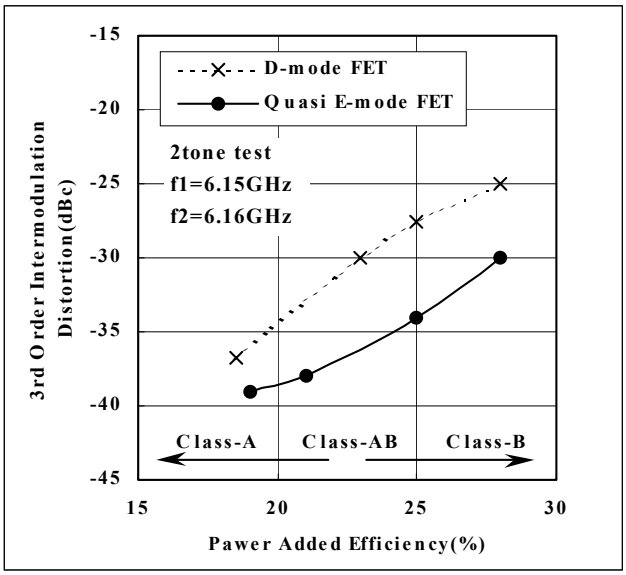

Fig.1. The comparison of IM_3 dependence on PAE for D-mode and quasi E-mode FET.
The average output power is 6 dB back-off from P_{sat}

DEVICE DESIGN

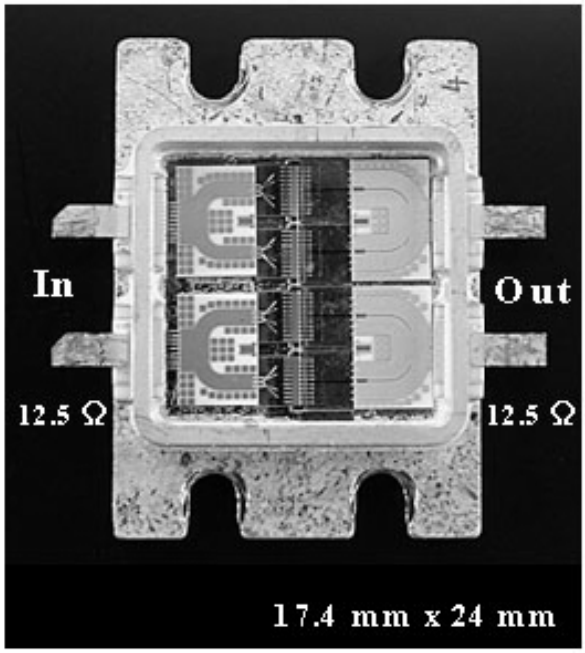

Fig.2. The Internal view of the 6 GHz, 50 Watt device.

The quasi E-mode FET has the advantage that IM_3 is better than D-mode FET at Class A-B operation.[2] Therefore, we decided to employ the quasi E-mode FETs for this application.

Fig.2 shows the internal view of 6 GHz, 50W device. This device consists of four 12 Watt chips which employ a quasi E-mode FET technology [2]. The gate length, the unit gate width and the total gate width of each chip is 0.6 μm, 240 μm and 28.8 mm, respectively. The package size is 17.4 x 24.0 mm.

Fig.3 shows the circuit network of the developed device. The input matching network consists of two stages of a lumped LC low pass filter network and single stage transmission line to obtain broad band frequency response. The output matching network consists of two stages of transmission line. The output matching circuit for each chip was designed to match maximum power added efficiency. This matching impedance was measured by load pull. The feed-through impedance of the package was designed to be 12.5 ohm. Parameters of input and output matching circuit were determined to transform chip impedance to 12.5 ohm. The input and the output matching circuit were simulated by the EM simulator to improve the accuracy. Furthermore, the quarter wave length impedance transformer from 12.5 ohm to 50 ohm and the 180degrees-hybrid-coupler were assembled on the test fixture external to the device.

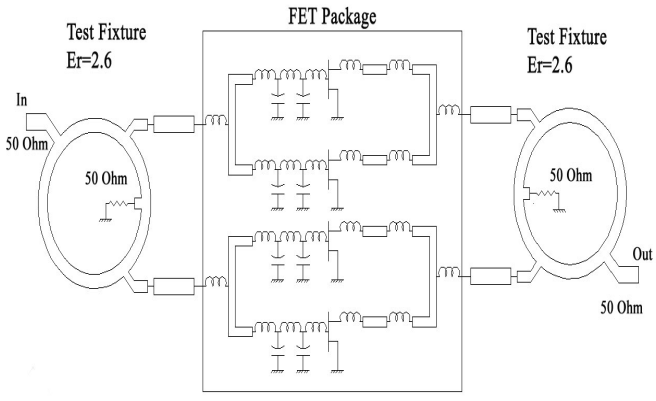

Fig.3. Matching network of the 6GHz 50watt push-pull FET

TEST FIXTURE DESIGN

The push-pull devices are generally used with coaxial baluns or multi-layer baluns for L- and S-band. However, a coaxial balun is very difficult to assemble, and multi-layer balun has a complex structure which is hard to fabricate.
Rat-race hybrid ring is one of the simplest ways to obtain the push-pull operation successfully at C-band. This Rat-race ring, which was fabricated with substrate of εr=2.6, had an insertion loss of 0.6 dB at 6GHz.

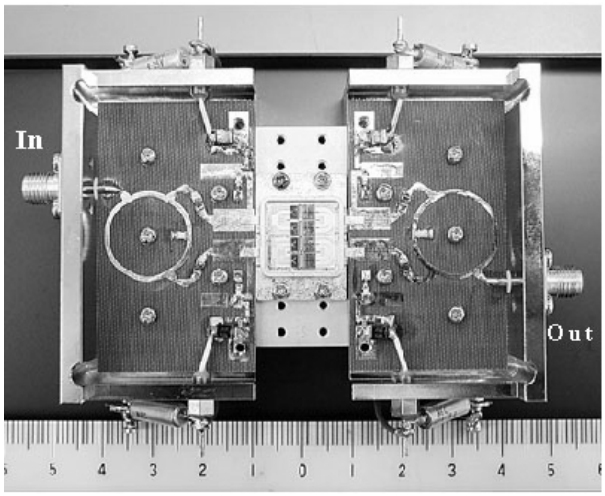

Fig.4. Test fixture drawing of the 6GHz 50Watt push-pull FET

THE PERFOMACE OF THE DEVICE

Fig.5 shows the measured output power and power-added efficiency at frequency of 5.8GHz to 6.5GHz. The FET was biased at V_{ds} of 12V and drain current (I_{ds}(DC)) of 5.0 A. A P_{sat} of 47dBm (50watt) was obtained with an associated power-added efficiency of 44% and G_L of 10dB.
Fig.6 shows frequency response of output power. Delta of linear gain (δ-G_L) was less than 0.6dB, and delta of P_{sat} was less than 0.3 dB. This device achieved excellent frequency response across 700MHz bandwidth.

In addition, the FET has a thermal resistance of 0.7 deg. C/W. A temperature rise from package to channel (δ-T_{ch}) is about 50 deg. C.

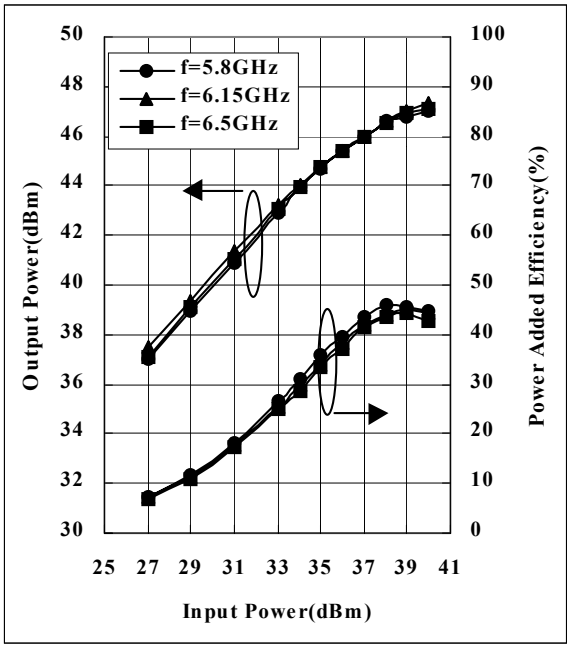

Fig.5. Output power and power-added efficiency versus input power

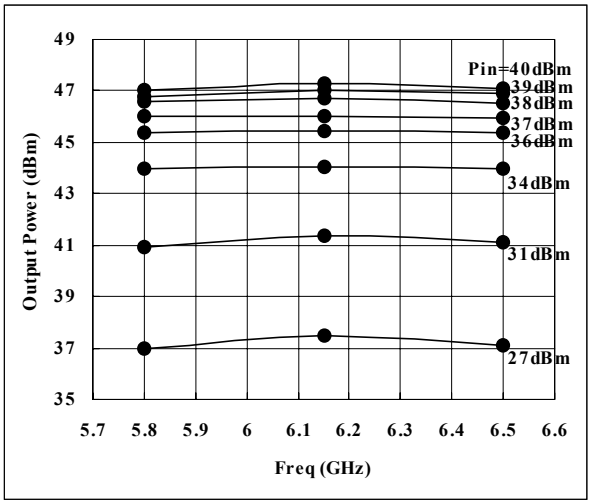

Fig.6 Frequency response of Output power

Fig.7 shows the measured IM_3 with 2-tone test. An IM3 of –35dBc with a power-added efficiency of 18% was obtained at an output power of 41dBm. As compared with

conventional D-mode single ended FET, an IM_3 and PAE improvement is 5dB and 5%, respectively.

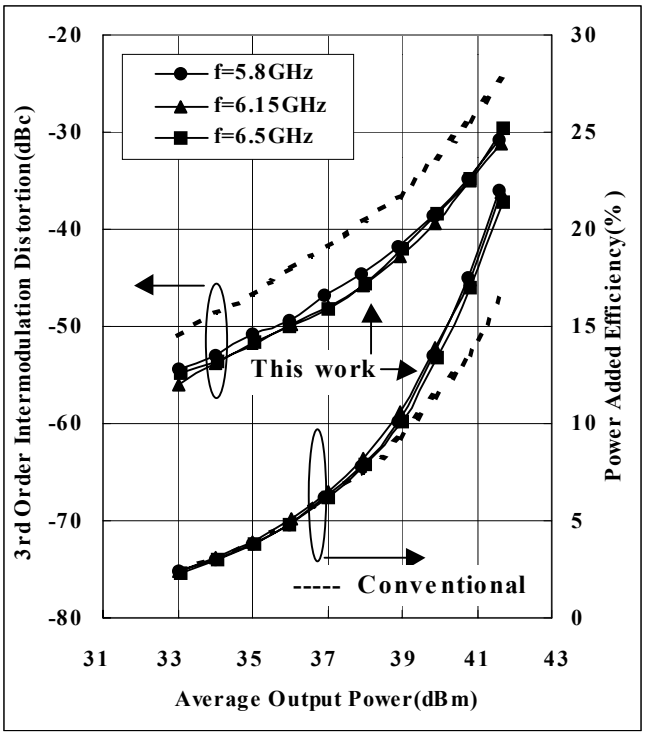

Fig.7. IM_3 and Power Added Efficiency versus Average output power

CONCLUSIONS

A 6 GHz 50 Watt GaAs push-pull FET has been developed with 44% power-added efficiency and at V_{ds} of 12V class A-B operation. An IM_3 of –35dBc with a power-added efficiency of 18% and a δ-T_{ch} of 50deg.C was obtained at an output power of 41dBm. Many C-band high capacity SDH radio link designs should benefit from this push-pull GaAs Power FET.

ACKOWLEDGMENT

The authors would like to acknowledge H.Takahashi, K.Inoue, K.Ebihara, and H.Haematsu for helpful discussion throughout this work, and I.Fukushima and W.Nakagomi for assistance in device assembly

REFERENCES

[1] K.Ebihara,H.Takahashi,Y.Tateno,T.Igarashi and J.Fukaya, “L-band 100-WATTs Push- Pull GaAs FET” 1998 MTT-S Digest, pp.703-706

[2] Y.Tateno,H.Takahashi,T.Igarashi and J.Fukaya, ”A 150W E-mode GaAs Power FET with 35% PAE for W-CDMA Base Station”1999 IEEE MTT-S Digest, pp.1087-1099

[3] K.Inoue,K.Ebihara,H.Haematsu,T.Igarashi and H.Takahashi, ”A 240W Push-PullGaAs Power FET for W-CDMA Base Station” 2000 IEEE MTT-S Digest, pp.1719-1722